

Appl. No. 10/605,419  
Amdt. dated May 12, 2005  
Reply to Office action of February 17, 2005

**Amendments to the Claims:**

**Listing of Claims:**

Claim 1 (original) A flash memory cell structure comprising:

a substrate having a stacked gate;

- 5       a select gate formed on the substrate and adjacent to one side of the  
stacked gate;  
a first-type doped region located in the substrate and adjacent to the  
select gate as a drain;  
a shallow second-type doped region located underneath the stacked  
10       gate and adjacent to the first-type doped region;  
a deep second-type doped region surrounding the first-type doped  
region and adjacent to the shallow second-type doped region; and  
a doped source region formed on a side of the shallow second-type  
doped region as a source.

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Claim 2 (original) The flash memory cell structure of claim 1 wherein a  
depth of the deep second-type doped region is deeper than a depth of the  
shallow second-type doped region.

- 20       Claim 3 (original) The flash memory cell structure of claim 1 wherein the  
deep second-type doped region has the same doped ions as the shallow  
second-type doped region.

- 25       Claim 4 (original) The flash memory cell structure of claim 3 wherein the  
doped ions of the deep second-type doped region and the shallow  
second-type doped region are selected from the III A group.

Claim 5 (original) The flash memory cell structure of claim 1 wherein the

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doped ions of the first-type doped region and the doped source region are selected from the V A group.

Claim 6 (original) The flash memory cell structure of claim 1 wherein the  
5 first-type doped region and the deep second-type doped region are electrically short-circuited together.

Claim 7 (original) The flash memory cell structure of claim 6 wherein the  
first-type doped region and the deep second-type doped region are  
10 electrically short-circuited by metal penetrating the junction between the first-type doped region and the deep second-type doped region.

Claim 8 (original) The flash memory cell structure of claim 6 wherein the  
first-type doped region and the deep second-type doped region are  
15 electrically short-circuited by metal exposed outside the first-type doped region and the deep second-type doped region of the substrate.

Claim 9 (original) The flash memory cell structure of claim 1 wherein the  
stacked gate includes a floating gate located over the shallow second-type  
20 doped region, and a control gate located over the floating gate.

Claims 10-16 (cancelled)

Claim 17 (new) A flash memory cell structure comprising:  
25 a substrate having a stacked gate;  
a select gate formed on the substrate and adjacent to one side of the stacked gate, the select gate being able to prevent an edge program

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disturb issue and an over program problem;  
a first-type doped region located in the substrate and adjacent to the  
select gate as a drain;  
a shallow second-type doped region located underneath the stacked  
5 gate and adjacent to the first-type doped region;  
a deep second-type doped region surrounding the first-type doped  
region and adjacent to the shallow second-type doped region; and  
a doped source region formed on a side of the shallow second-type  
doped region as a source.

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Claim 18 (new) The flash memory cell structure of claim 17 wherein a  
depth of the deep second-type doped region is deeper than a depth of the  
shallow second-type doped region.

15 Claim 19 (new) The flash memory cell structure of claim 17 wherein the  
deep second-type doped region has the same doped ions as the shallow  
second-type doped region.

Claim 20 (new) The flash memory cell structure of claim 19 wherein the  
20 doped ions of the deep second-type doped region and the shallow  
second-type doped region are selected from the III A group.

Claim 21 (new) The flash memory cell structure of claim 17 wherein the  
doped ions of the first-type doped region and the doped source region are  
25 selected from the V A group.

Claim 22 (new) The flash memory cell structure of claim 17 wherein the  
first-type doped region and the deep second-type doped region are

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electrically short-circuited together.

Claim 23 (new) The flash memory cell structure of claim 22 wherein the first-type doped region and the deep second-type doped region are  
5 electrically short-circuited by metal penetrating the junction between the first-type doped region and the deep second-type doped region.

Claim 24 (new) The flash memory cell structure of claim 22 wherein the first-type doped region and the deep second-type doped region are  
10 electrically short-circuited by metal exposed outside the first-type doped region and the deep second-type doped region of the substrate.

Claim 25 (new) The flash memory cell structure of claim 17 wherein the stacked gate includes a floating gate located over the shallow second-type  
15 doped region, and a control gate located over the floating gate.